

AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please add new claims 15-20.

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1. (CURRENTLY AMENDED) A method of conditional branching in a pipelined processor, the method comprising the steps of:

5 (A) prefetching fetching a first instruction stored at
a branch target address in response to encountering a branch instruction, ~~in prediction of taking a branch at a program counter~~
~~address; and~~

10 (B) decoding a second instruction stored at a next
address adjacent said program counter address substantially
simultaneously with said fetching; and

15 (C) evaluating between (i) taking said a branch defined
by said branch instruction and (ii) not taking said branch
substantially simultaneously with said fetching contemporaneously
with prefetching said branch target address.

2. (CURRENTLY AMENDED) The method of claim 1, further comprising the steps of:

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prefetching fetching a third instruction stored at a
sequential instruction address adjacent said branch target address
5 in response to evaluating determining to take said branch, or
~~prefetching a mispredict recovery address in response to~~
~~evaluating not taking said branch.~~

3. (CURRENTLY AMENDED) The method of claim 2, further comprising the step of:

generating said sequential instruction address based upon
a said program counter address and a predetermined offset.

4. (CURRENTLY AMENDED) The method of claim 2, further comprising the step of:

generating said misprediction recovery address based upon
an exception program counter address and a second predetermined
5 offset.

5. (CURRENTLY AMENDED) The method of claim 1, further comprising the step of:

generating said branch target address based upon a said
program counter address and an address displacement of said branch
5 condition instruction.

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6. (CURRENTLY AMENDED) The method of claim 1, further comprising the steps of:

generating a sequential instruction address adjacent said branch target address based upon a said program counter address and 5 a first predetermined offset;

generating a misprediction mispredict recovery address adjacent said next address based upon an exception program counter address and a second predetermined offset;

generating said branch target address based upon a said 10 program counter address and an address displacement of said branch condition instruction;

prefetching fetching a third instruction stored at said sequential instruction address in response to evaluating 15 determining to take said branch; and

prefetching fetching a fourth instruction stored at said mispredict recovery address in response to evaluating not taking determining to not take said branch.

7. (CURRENTLY AMENDED) A pipelined processor comprising:

a multiplexer; and

a circuit configured to present (i) a branch target 5 address based on a branch instruction stored at a program counter address to said multiplexer in prediction of taking a branch, (ii)

a sequential instruction address having a first value adjacent said program counter address and (ii) (iii) a mispredict recovery address to said multiplexer when not taking said branch substantially simultaneously.

8. (CURRENTLY AMENDED) The pipelined processor of claim 7, wherein said circuit is further configured to present a sequential instruction address having a second value adjacent said branch target address to said multiplexer when taking said branch in response to determining to take said branch.

9. (CURRENTLY AMENDED) The pipelined processor of claim 7, further comprising wherein said circuit comprises:

a prefetch program counter for storing a program counter an address presented by said multiplexer among said branch target address, said sequential instruction address and said misdirect recovery address and used in generating said sequential instruction address.

10. (CURRENTLY AMENDED) The pipelined processor of claim 7, further comprising wherein said circuit comprises:

a prefetch program counter for storing a program counter address presented by said multiplexer and used in generating said branch target address, and

an instruction register for storing said branch instruction used in generating said branch target address.

11. (CURRENTLY AMENDED) The pipelined processor of claim 7, ~~further comprising wherein said circuit comprises:~~

an exception program counter disposed in a decode stage of said pipelined processor for storing an exception program counter address used ~~in generating said mispredict recovery address upon determining not to take said branch.~~

12. (CURRENTLY AMENDED) The pipelined processor of claim 7, ~~further comprising wherein said circuit comprises:~~

an exception program counter disposed in an execution stage of said pipelined processor for storing an exception program counter address used ~~in generating said mispredict recovery address upon determining not to take said branch.~~

13. (CURRENTLY AMENDED) The pipelined processor of claim 7, ~~further comprising: wherein said circuit comprises:~~

~~said circuit being further configured to provide a sequential instruction address to said multiplexer for use upon choosing to take said branch,~~

a prefetch program counter for storing ~~a~~ said program counter address presented by ~~said~~ multiplexer and used in

~~generating said sequential instruction address and said branch target address;~~

10 an instruction register for storing said branch instruction ~~used in generating said branch target address~~; and
 an exception program counter for storing an exception program counter address used in generating said mispredict recovery address having a second value proximate said program counter address.

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14. (CURRENTLY AMENDED) A pipelined processor comprising;

a means for multiplexing decoding a first instruction stored at a next address adjacent a program counter address;

5 a means for presenting fetching a second instruction stored at a branch target address to said means for multiplexing in prediction of taking substantially simultaneously with said decoding in response to encountering a branch instruction at said program counter address; and

10 a means for presenting a mispredict recovery address to said means for multiplexing when evaluating between (i) taking a branch defined by said branch instruction and (ii) not taking said branch substantially simultaneously with said fetching.

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15. (NEW) The method of claim 1, further comprising the
step of:

fetching a third instruction stored at a mispredict
recovery address adjacent said next address in response to
5 determining not to take said branch.

16. (NEW) The method of claim 1, further comprising the
step of:

storing said program counter address in a stage of said
pipelined processor for at least two cycles.

17. (NEW) The pipelined processor of claim 13, wherein
said circuit further comprises:

an incrementor coupled to said prefetch program counter
and configured to generate said sequential instruction address from
5 said program counter address.

18. (NEW) The pipelined processor of claim 13, wherein
said circuit further comprises:

an adder (i) coupled to both said prefetch program
counter and said instruction register and (ii) configured to
5 generate said branch target address by adding said program counter
address to an address displacement of said branch instruction.

19. (NEW) The pipelined processor of claim 13, wherein
said circuit further comprises:

an incrementor coupled to said exception program counter
and configured to generate said mispredict recovery address.

20. (NEW) The pipelined processor of claim 13, wherein
said exception program counter is coupled to said prefetch program
counter to receive said program counter address.